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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,940	08/28/2003	Katsuhiko Oyama	04329.3125	6236

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
LUU, CHUONG A	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,940	OYAMA, KATSUHIKO	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 23 June 2005.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) 18-31 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The Rejections

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Tokuno et al. (U.S. 5,883,426).

Tokuno discloses a stack module with

(1); (6); (12) a plurality of semiconductor chips (1) having a plurality of terminals (6);

two chip mounting bases (2d, 3) on each of which one semiconductor chips (1) mounted and plurality of chip interconnections electrically least connected the terminals

mounted semiconductor chip (1) are formed into substantially the same pattern and which are stacked two layers along a direction thickness;

one between interconnection base which is interposed two chip mounting bases (2d, 3) and on which a plurality of intermediate interconnections electrically connected to the chip interconnections are formed into a pattern different from the pattern the chip interconnections (6);

a plurality of interlevel interconnections which are formed a plurality of through holes extending through the chip mounting bases and the interconnection base at once along stacking direction and electrically connect the chip interconnections and intermediate interconnections the stacking direction the bases (see Figures 1-2);

(2) wherein: the chip interconnections and the intermediate interconnections are formed on facing major surfaces of at least one of the two chip mounting bases and the interconnection base (see Figures 1-2);

(3); (9); (15) wherein: the through holes extend through feedthrough terminals the chip interconnections and the intermediate interconnections (see Figures 1-2);

(4); (10); (16) wherein: the intermediate interconnections are formed into a pattern capable of setting signal paths from the terminals independently for each terminal and each layer (see Figures 1-2);

(5); (11); (17) wherein: the intermediate interconnections are formed a pattern capable of switching, between the layers for each terminal, signal paths between the terminals and a plurality of external terminals which externally electrically connect the semiconductor chips (see Figures 1-2);

(7); (13) wherein: the chip interconnections and the intermediate interconnections are formed on facing major surfaces of the bases for a pair of at least one of the two chip mounting bases and the first second base adjacent chip mounting base;

(8) wherein: the chip interconnections and the intermediate interconnections are formed on facing major surfaces the bases a pair of one of the two chip mounting bases and the first interconnection base and a pair of the other chip mounting base and the second interconnection base;

(14) wherein: the number of interconnection bases equal to the number of chip mounting bases are arranged, and the chip interconnections and the intermediate interconnections are formed on facing major surfaces of the bases for all pairs of the chip mountlng bases and the interconnection bases adjacent to the chip mounting bases (see Figures 1-2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
September 6, 2005